slanted, the second surface forming an angle of between 5 and 85 degrees with the surface of the III-N material structure.

33. The device of claim **1**, wherein the extending portion directly contacts the sidewall.

34. A III-N semiconductor device, comprising:

an electrode-defining layer having a thickness on a surface of a III-N material structure, the electrode-defining layer having a recess with a sidewall, the sidewall comprising a plurality of steps, wherein a portion of the recess distal from the III-N material structure has a first width, and a portion of the recess proximal to the III-N material structure has a second width, the first width being larger than the second width; and

an electrode in the recess, the electrode including an extending portion over the sidewall, a portion of the electrode-defining layer being between the extending portion and the III-N material structure; wherein

at least one of the steps in the sidewall has a first surface that is substantially parallel to the surface of the III-N material structure and a second surface that is slanted, the second surface forming an angle of between 5 and 85 degrees with the surface of the III-N material structure.

35. The device of claim **34**, wherein the III-N material structure comprises a first III-N material layer and a second III-N material layer, wherein a 2DEG channel is induced in the first III-N material layer adjacent to the second III-N material layer as a result of a compositional difference between the first III-N material layer and the second III-N material layer.

36. The device of claim **35**, wherein the first III-N material layer includes GaN.

37. The device of claim **36**, wherein the second III-N material layer includes AlGaN or AlInGaN.

38. The device of claim **35**, further including a third III-N material layer between the first III-N material layer and the second III-N material layer.

39. The device of claim **38**, wherein the third III-N material layer comprises AlN.

40. The device of claim **35**, wherein the first III-N material layer and the second III-N material layer are group III-face or [0 0 0 1] oriented or group-III terminated semipolar layers, and the second III-N material layer is between the first III-N material layer and the electrode-defining layer.

41. The device of claim **35**, wherein the first III-N material layer and the second III-N material layer are N-face or [0 0 0 1 bar] oriented or nitrogen-terminated semipolar layers, and the first III-N material layer is between the second III-N material layer and the electrode-defining layer.

42. The device of claim **35**, wherein the recess extends through the entire thickness of the electrode-defining layer.

43. The device of claim **42**, wherein the recess extends into the III-N material structure.

44. The device of claim **43**, wherein the recess extends through the 2DEG channel.

45. The device of claim **43**, wherein the recess extends at least 30 nanometers into the III-N material structure.

46. The device of claim **34**, wherein the recess extends partially through the thickness of the electrode-defining layer.

47. The device of claim **34**, wherein the electrode-defining layer has a composition that is substantially uniform throughout.

48. The device of claim **34**, wherein the electrode-defining layer comprises SiN_x.

49. The device of claim **34**, wherein a thickness of the electrode-defining layer is between about 0.1 microns and 5 microns.

50. The device of claim **34**, further comprising a dielectric passivation layer between the III-N material structure and the electrode-defining layer, the dielectric passivation layer directly contacting a surface of the III-N material adjacent to the electrode.

51. The device of claim **50**, wherein the dielectric passivation layer comprises SiN_x.

52. The device of claim **50**, wherein the dielectric passivation layer is between the electrode and the III-N material structure, such that the electrode does not directly contact the III-N material structure.

53. The device of claim **50**, further comprising an additional insulating layer between the dielectric passivation layer and the electrode-defining layer.

54. The device of claim **53**, wherein the additional insulating layer comprises AlN.

55. The device of claim **53**, wherein the additional insulating layer is less than about 20 nanometers thick.

56. The device of claim **34**, wherein the extending portion of the electrode functions as a field plate.

57. The device of claim **34**, wherein the electrode is an anode, and the device is a diode.

58. The device of claim **34**, wherein the electrode is a gate, and the device is a transistor.

59. The device of claim **58**, wherein the device is an enhancement-mode device.

60. The device of claim **58**, wherein the device is a depletion-mode device.

61. The device of claim **34**, wherein the device is a high-voltage device.

62. The device of claim **34**, wherein the extending portion directly contacts the sidewall.

63. A method of forming a III-N device, comprising:

forming an electrode-defining layer having a thickness on a surface of a III-N material structure;

patterning a masking layer over the electrode-defining layer, the masking layer including an opening having a width;

etching the electrode-defining layer to form a recess therein, the recess having a sidewall which comprises a plurality of steps, a portion of the recess distal from the III-N material structure having a first width, and a portion of the recess proximal to the III-N material structure having a second width, the first width being larger than the second width;

removing the masking layer; and

forming an electrode in the recess, the electrode including an extending portion over the sidewall, a portion of the electrode-defining layer being between the extending portion and the III-N material structure; wherein

the etching step includes a first procedure and a second procedure, the first procedure comprising removing a portion of the electrode-defining layer, and the second procedure comprising removing a portion of the masking layer without entirely removing the masking layer, the second procedure causing an increase in the width of the opening in the masking layer.

64. The method of claim **63**, wherein the first procedure is performed a second time after the second procedure has been performed.